

# Mechanical stress evolution in metal interconnects for various line aspect ratios and passivation dielectrics

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## Abstract

Both X-ray diffraction and finite element analyses were used to investigate the effects of various passivation dielectrics and metal line aspect ratios on the mechanical stress in Al–Cu interconnect lines. Volume-averaged stresses were measured and calculated by considering not only residual stresses and mechanical properties of passivation dielectrics but also their characteristic deposition shapes. Interconnect stress increased with increasing passivation stiffness and line aspect ratio due to the normal constraint by passivation dielectrics, while it was relaxed in narrow lines passivated with voided or air-gapped dielectrics. A reasonable correlation between the measured and calculated stresses was found when void or gap in dielectric between metal lines was taken into account in numerical analysis.

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## 1. Introduction

The reliability of microelectronic devices is strongly influenced by thermal stresses developed in the multilevel interconnect structures. The incorporation of several levels of metallization and passivation in an integrated circuit device exposes the interconnects to multiple thermal cycles as much as 400 °C. High tensile stresses evolve in the metal lines on cooling from the passivation temperature by the thermal expansion mismatches with the surrounding dielectrics and Si substrate. These triaxial tensile stresses that arise within the lines facilitate void formation, which can eventually cause the failure of devices [1,2]. Therefore, precise measurement and thorough understanding of interconnect stress are essential to ensure the device reliability.

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Dielectric passivation on metal interconnect can significantly change the stress–state in the metal line [3–6]. Different stress states in the conductor lines by different passivation materials would strongly influence the stress-induced voiding [7,8]. Finite element method (FEM), curvature measurement method, and X-ray diffraction (XRD) method have been used to evaluate the effects of passivation on the stress evolution in metal interconnects [3–10]. Systematic XRD stress measurement results showed that the effect of passivation stress on the metal interconnect stress was not large [11]. It was shown that interconnect stress increased with increasing passivation stiffness by finite element stress calculation [6,7] and also XRD stress measurements [8–12]. Although, in addition to the mechanical properties of passivation materials, both characteristic deposition shape of passivation dielectric and void or air-gap existence would significantly influence the interconnect stress, only a few results [13,14] reported that passivation stiffness and geometry affected the interconnect stress for 1  $\mu\text{m}$  width/space Al line arrays. By the way, increase in line aspect ratio (defined by line thickness divided by line width) due to the decreased line width used in integrated circuit devices significantly affects thermal stress evolutions in metal interconnect. Systematic finite element analysis [6] showed that the volume-averaged stress of Al lines increased with increasing line aspect ratio until the aspect ratio became one, and then decreased beyond that value. These results could be applicable only for a passivated single (or, isolated) Al line on a substrate [4,6]. However, narrow metal lines are generally densely arrayed in actual integrated circuit devices, for example, using sub-0.2- $\mu\text{m}$  for metal line width and space in current standard logic devices. Although there have been some numerical [4–6] and analytical [9] results on the effects of line aspect ratio in the periodic array of metal lines passivated with ideal oxide, experimental results on the effects of line aspect ratio have not been explicitly explored for actual dielectric materials currently used in industry. Also, as noted earlier, the characteristic deposition shape of dielectric and void existence should be considered in order to understand the exact stress state in passivated narrow lines. We used both direct XRD analysis and finite element analysis to investigate the effects of various passivation dielectrics and metal line aspect ratios on mechanical stress-state in Al–Cu interconnects. Passivation dielectrics used in this study were PETEOS (plasma enhanced tetra ethyl ortho silicate), FOx (flowable oxide), HDP FSG (high-density plasma fluorinated silicate glass), and PE-SiN (plasma enhanced-silicon nitride). A series of parallel interconnect lines with various aspect ratios at a constant pattern density of 50% were used for stress analysis. Plane-strain, elasto-plastic finite element analyses were carried out to calculate thermal stress by using Young’s modulus of each constituent layer of metal stack measured by the nanoindentation method. Finally, volume-averaged stresses from finite element analysis were compared to experimentally measured estimates by considering not only the mechanical properties of passivation dielectrics but also their characteristic deposition shapes.

## 2. Experimental and numerical procedures

Test structure with one-level metallization as shown in Fig. 1 was fabricated using the procedure described below. 100-nm thick PETEOS was deposited on a P-type  $\langle 100 \rangle$ Si wafer. A bottom-Ti (10 nm)|Al–0.5%Cu (350 nm)|Ti (5 nm)|TiN (60 nm)-top stack was then deposited using a multichamber dc magnetron sputtering system without a vacuum break. That is, 10 nm of Ti was deposited, followed by in situ sputter deposition of 350 nm of Al–0.5%Cu with a process power of 12 KW at 400 °C. On the top of the Ti|Al structure, 5 nm of Ti and 60 nm of TiN were deposited in a single

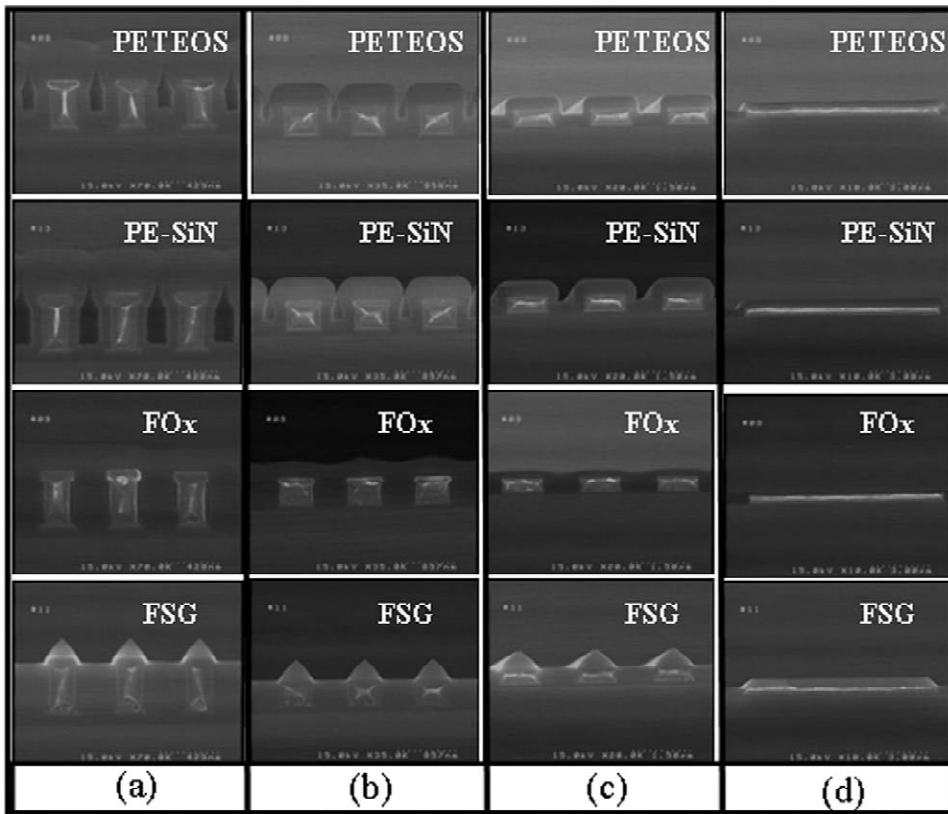


Fig. 1. Cross-sectional SEM photograph of periodically arrayed Al lines passivated by different dielectrics for  $w/h$ : (a) 0.6 (line width/space:  $0.25\ \mu\text{m}/0.25\ \mu\text{m}$ ), (b) 1.2 ( $0.5\ \mu\text{m}/0.5\ \mu\text{m}$ ), (c) 2.4 ( $1\ \mu\text{m}/1\ \mu\text{m}$ ), and (d) 23.5 ( $10\ \mu\text{m}/10\ \mu\text{m}$ ).

chamber. The metal stack was then patterned by standard photolithography and plasma dry etching. One of four kinds of dielectric layers, 450-nm thick, was deposited on the patterned lines; plasma enhanced CVD (chemical vapor deposition) oxide with a TEOS source (PETEOS), flowable oxide by spin coating (FOx or HSQ [hydrogen silses quioxane]), high-density plasma CVD oxide with fluorine (HDP FSG or FSG), and plasma enhanced CVD nitride (PE-SiN). Four different  $4000\ \mu\text{m}$  long-periodic straight metal lines with the same width and space were made in four different  $4 \times 4\ \text{mm}^2$  square blocks. Selected line widths,  $w$  (and the same spaces,  $s$ ) were  $0.25\ \mu\text{m}$ ,  $0.5\ \mu\text{m}$ ,  $1\ \mu\text{m}$ , and  $10\ \mu\text{m}$  which correspond to an inverse aspect ratio ( $w/h$ ) of 0.6, 1.2, 2.4, and 23.5, respectively (height,  $h$ , is  $0.425\ \mu\text{m}$ , that is, thickness of Ti|Al–Cu|Ti|TiN stack) as shown in Fig. 1. It could be observed that PETEOS and PE-SiN samples had void channels between metal lines connected from the metal bottom surface or metal middle position to the oxide top surface for  $w/h = 0.6$  and  $w/h = 1.2$ . There was no void or air gap in FSG and FOx for all  $w/h$  values. These voids or gaps in oxide between metal lines could affect the interconnect stress which was investigated in detail in this study. Young's modulus and residual stress of every constituent layer used in this test structure were measured on a Si wafer by the nanoindentation method [15] and wafer curvature method, respectively. Data measured at five different positions of each sample were averaged to give Young's modulus of

each layer. The XRD experiment was done with a monochromated Cu K $\alpha$  beam, at 40 kV and 100 mA conditions. The X-ray beam was aligned to expose the center of each 4  $\times$  4 mm<sup>2</sup> square block composed of uniform line and space patterns. We measured {422} lattice spacing of Al interconnect passivated with various dielectrics along the parallel and perpendicular directions of a dense array of straight Al lines. From these XRD experimental results, the triaxial components of lattice spacing ( $d$ ), strain ( $\epsilon$ ), and stress ( $\sigma$ ) of Al interconnect were obtained separately in length ( $x$ ), width ( $y$ ), and height ( $z$ ) direction. Detailed procedures to calculate Al interconnect stress were explained in several Refs. [3,11,16,17]. With this technique, the stress of the blanket Al film was also compared with that of the blanket Al stack film (bottom-Ti|Al-0.5%Cu|Ti|TiN-top) with or without passivation dielectrics.

To model the actual geometry with a periodic nature of line structure, only the right half of the unit segment (cf. Fig. 2 for PETEOS or PE-SiN with  $w/h=0.6$ ) was used by setting the displacement ( $v$ ) in the  $y$  direction to vanish along the metal line center to ensure symmetry condition. The top surface was free to move during deformation. The surface of the oxide layers above the Al lines was kept flat. The thickness of these layers above the Al line is 450 nm. We assumed a rectangular shape of FSG directly above the Al line because there was just a little difference in calculated Al stress between the cone shape (cf. Fig. 1) and the rectangular shape of FSG (cf. Fig. 2). The only differences were the lateral boundary conditions which were illustrated for only one case in Fig. 2. In case there was a void channel between metal lines connected from the metal bottom surface to the oxide top surface (cf.,

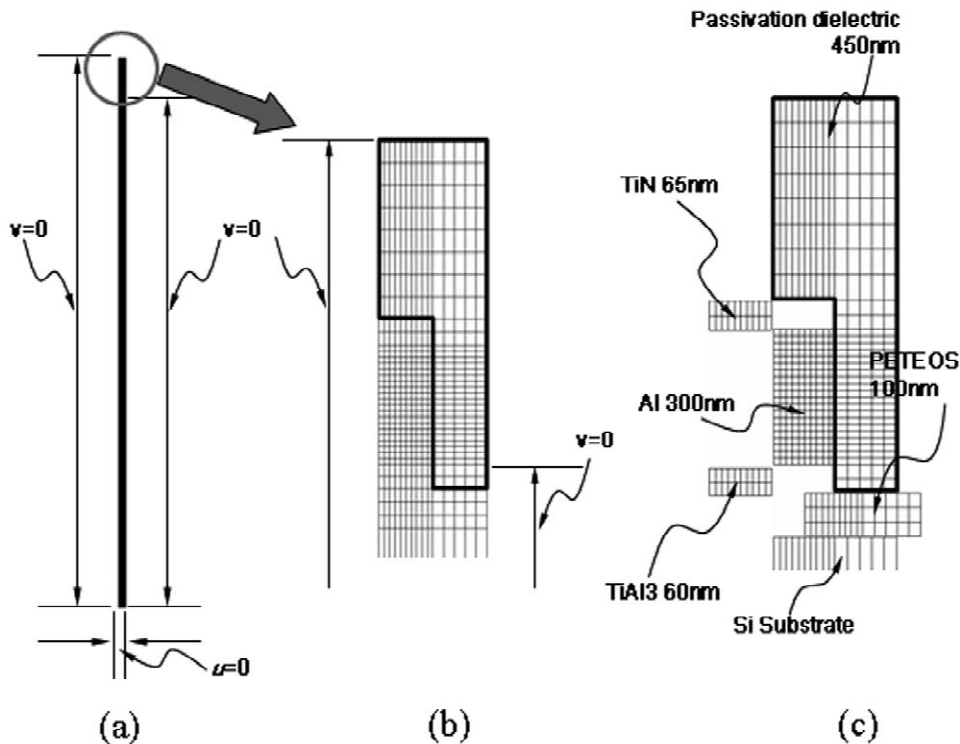


Fig. 2. Finite element mesh of the right half of unit metal line structure. Boundary conditions are represented for PE-SiN passivation and  $w/h=0.6$  where  $u$  and  $v$  are the displacement in line thickness and width direction, respectively: (a) finite element mesh, (b) zoomed mesh around the metal line, (c) constituent materials in the zoomed mesh.

Table 1  
Material properties used in the finite element analysis

Material	$E$ (GPa)	$\nu$	CTE (ppm/K)	Yield stress (MPa)
Si	145	0.26	2.6	
Al–Cu	59–0.04 ( $T-20\text{ }^{\circ}\text{C}$ )	0.34	24.3 + 0.02 ( $T-20\text{ }^{\circ}\text{C}$ )	200–0.35 ( $T-20\text{ }^{\circ}\text{C}$ )
TiN	270	0.25	9.4	
FSG	51	0.19	3	
FOx	8	0.19	20.5	
PETEOS	75	0.24	1	
PE-SiN	203	0.25	1	

PE-SiN with  $w/h=0.6$ ), the side walls were allowed to move freely, as shown in Fig. 2. In case there was no void or gap between metal lines (cf., FOx and FSG with the whole range of aspect ratio), no displacement ( $v$ ) was allowed in the  $y$  direction along the whole side walls. Where there was a void channel between metal lines connected from the metal middle position to the oxide top surface (cf. PE-SiN with  $w/h=1.2$  or PETEOS with  $w/h=0.6, 1.2$ ), the voided part of the side wall was allowed to move freely while no displacement was allowed in the  $y$  direction along the lower part (that is, below the metal line middle position). Where there was a gap from the metal top surface to the oxide top surface (cf. PE-SiN or PETEOS with  $w/h=2.4, 23.5$ ), the air-gapped part of the side wall was allowed to move freely while no displacement was allowed in the  $y$  direction along the lower part (that is, below metal line top surface). The general purpose finite element program ABAQUS [18] was used to calculate the stress distributions in the model structure assuming a good adhesion between dissimilar materials and a uniform temperature distribution in the model structure at each temperature step. In addition, stress-free state of the model was assumed to be the dielectric deposition temperature (roughly  $400\text{ }^{\circ}\text{C}$ ). The intrinsic stress of each constituent material was ignored, based on the assumption that it could be considered to have been fully relaxed at the dielectric deposition temperature, which was reported in some earlier works [1–3]. Therefore, the stress calculated in this study was the thermal stress induced by thermal expansion mismatches between dissimilar materials during cooling from the initial stress-free temperature ( $400\text{ }^{\circ}\text{C}$ ) to room temperature ( $25\text{ }^{\circ}\text{C}$ ). Eight-noded isoparametric plane strain elements were used to make up the finite element mesh. Al–Cu was assumed to behave as an elastic-plastic material while the other layers have linear-elastic behavior. Temperature-dependent material properties were also used for Al–Cu [2–6]. Table 1 summarizes the material properties used in this simulation where each value of Young's modulus at room temperature was measured by the nanoindentation method and the others taken from [2–6]. Due to lack of mechanical property data of thin ( $\sim 60\text{ nm}$ )  $\text{TiAl}_3$  layer (cf. Fig. 2) formed under Al–Cu line [19–21], we used the measured Young's modulus of TiN as that of  $\text{TiAl}_3$  in finite element simulation. Convergence of the finite element results was checked through various degrees of mesh refinement to get the important features of stress distributions in the metal interconnect.

### 3. Results and discussion

It is very important to use the correct mechanical properties of each constituent material used in this structure to calculate the accurate mechanical stress of metal interconnect. Young's modulus and

residual stress of every constituent layer used in this test structure (cf. Fig. 1 or 2) were measured with a blanket film by the nanoindentation and the wafer curvature method, respectively (cf. Table 1). Fig. 3 compares Young's modulus ( $E$ ), coefficient of thermal expansion (CTE), and residual stress of four different passivation dielectrics. Young's modulus of oxide decreased from PE-SiN, PETEOS, FSG, and FOx while the residual stress did not show a clear consistency with these stiffness trends. CTE in the literature [2–6] showed roughly opposite trends to the measured Young's modulus. Although plasma deposited films, such as PE-SiN and PETEOS, are expected to be less dense than HDP films, adding fluorine to an HDP film (FSG HDP) seemed to make the film less stiff than the plasma deposited film.

Measurement of residual stress of the Al–Cu interconnect using XRD methods requires the lattice spacing of unstressed Al–Cu film [3,16,17]. Due to the strong (111) texture of the Al–Cu film, especially on Ti underlayers [19,20], only two different type {422} planes near the  $\sin^2 \Psi$  of 0.11 and 0.78 could be observed, where  $\Psi$  indicates the angle from the sample normal to the normal of a diffracting plane [3,16,17]. Lattice spacing of the Al {422} plane without stress ( $d_0$ ) was obtained

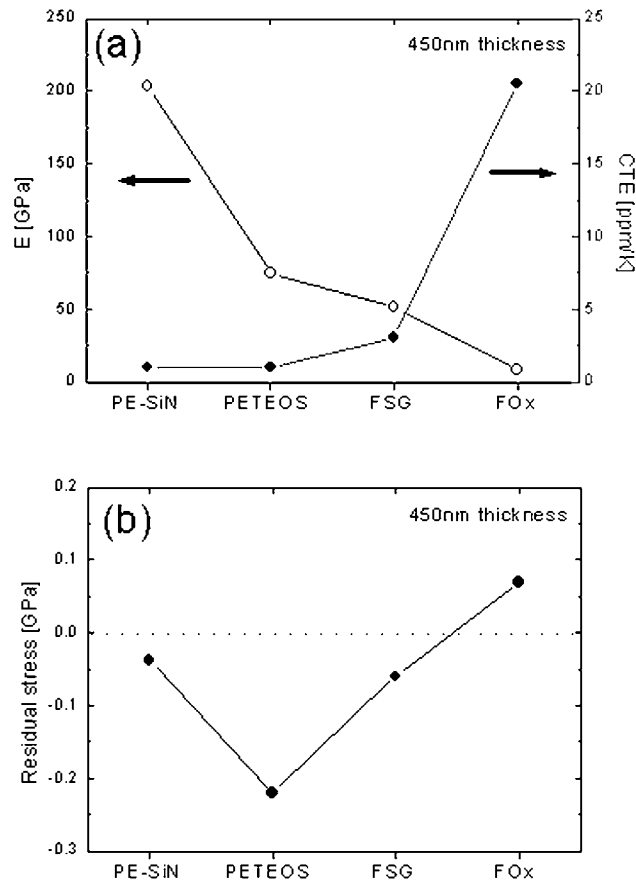


Fig. 3. Comparison of (a) Young's modulus ( $E$ ), coefficient of thermal expansion (CTE), and (b) residual stress of different dielectric films with 450-nm thickness.

from a blanket Al film and a blanket Al stack film (bottom-Ti|Al-0.5%Cu|Ti|TiN-top) with or without various passivation dielectrics as shown in Fig. 4. Measured  $d_0$  was 0.0826654 nm, which agreed well with the reported results [8,17]. An Al film without Ti underlayer showed a different stress state compared to that with Ti underlayer while passivation did not affect the blanket Al film stress. The increment of stress in an underlying metal film by passivation film is negligible because stress in a given metal film depends only on its misfit with the substrate. It was reported that a Ti–Al reaction layer ( $\text{TiAl}_3$ ) was uniformly formed across the bottom-Ti|Al interface during normal fabrication, which was accompanied by a 5–6% volume shrinkage [20,21]. So, the remaining Al experiences a tensile strain in the out-of-plane direction ( $z$ , film normal direction), leading to a compressive strain in the in-plane direction ( $x$  or  $y$ , film parallel direction). This resulted in the smaller in-plane stress of Al film with Ti underlayer compared to that without Ti underlayer. Triaxial stress components ( $\sigma_x, \sigma_y, \sigma_z$ ) and hydrostatic stress [ $\sigma_h = (\sigma_x + \sigma_y + \sigma_z)/3$ ] of Al interconnects were

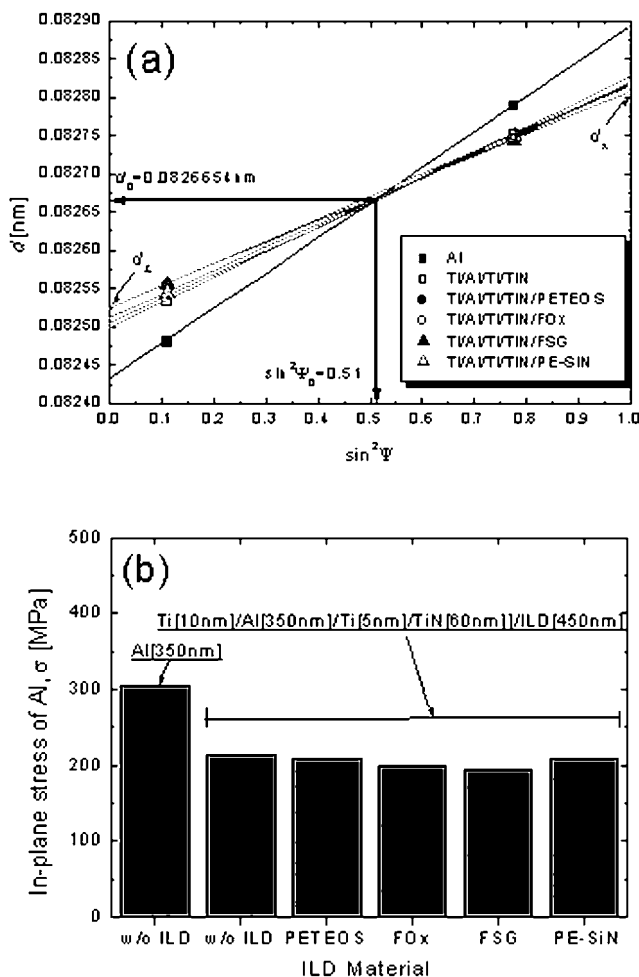


Fig. 4. (a) Al {422} interplanar spacings as a function of  $\sin^2 \Psi$  for blanket Al film and Al stack film (bottom-Ti|Al-0.5%Cu|Ti|TiN-top) with or without various passivation dielectrics, (b) XRD-measured in-plane stress of each Al film.

measured for various passivation dielectrics. Measured stress data were compared to the calculated values for patterned and nonpatterned Al, as shown in Table 2, which will be discussed later in detail.

To obtain the overall trend on the effects of line aspect ratio and passivation material and to compare these with the measured stress, only volume-averaged stresses calculated from stress distribution data inside Al line obtained by FEM were shown here. The calculated average stress components in periodically arrayed Al lines as a function of  $w/h$  were shown for various passivation dielectrics in Fig. 5. It could be seen that the interconnect stresses for FSG, PETEOS, and PE-SiN increased monotonically with decreasing  $w/h$  (or, increasing line aspect ratio) from 23.5 to 1.2, and then FSG showed a further increase while PETEOS and PE-SiN showed a sharp decrease at  $w/h=0.6$ . FOx had nearly constant stresses for large variations of  $w/h$ . Therefore, for  $w/h>1.2$ , line stress increased with an increasing line aspect ratio due to the normal constraint by stiff passivation dielectric while for FOx it increased just a little due to its very low stiffness (cf. 3). FSG and FOx had no void or air gap between metal lines for  $w/h<1.2$  (cf. Fig. 1), so we used the constrained side boundary conditions which resulted in continuous stress increase with little stress relaxation. Because PETEOS and PE-SiN had a void channel between metal lines for  $w/h<1.2$  (cf. Fig. 1), we used the unconstrained side boundary conditions (cf. Fig. 2 for PE-SiN with  $w/h=0.6$ ), which led to large stress relaxation due to the reduced transverse constraint in the narrowest lines. Calculations of interconnect stresses using unsuitable boundary conditions (cf. constrained or unconstrained side wall) could lead to false results, especially for narrow line structures, as emphasized in Ref. [4]. It is clear that using proper dielectric deposition shape (cf. with or without void or gap in the oxide), accurate

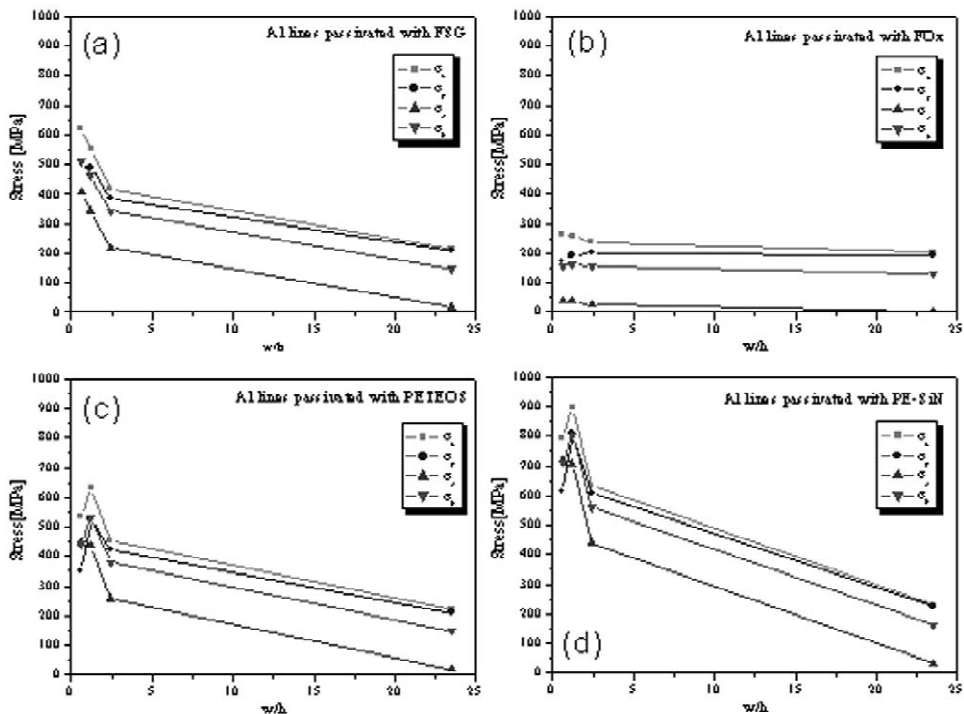


Fig. 5. Calculated volume-averaged stress components in periodically arrayed Al lines as a function of  $w/h$  for various passivation dielectrics: (a) FSG, (b) FOx, (c) PETEOS and (d) PE-SiN.

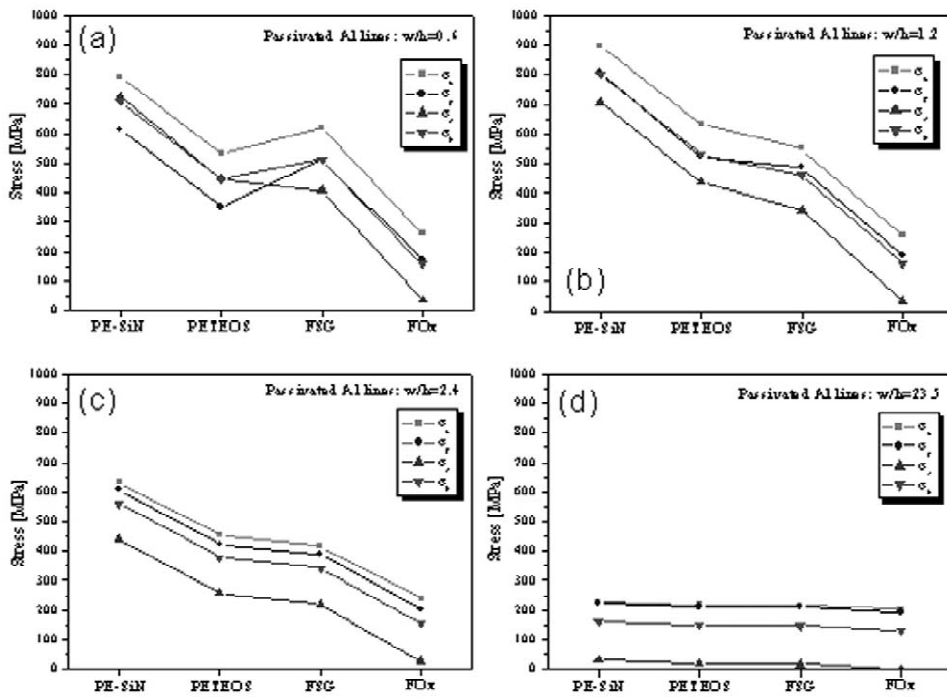


Fig. 6. Calculated volume-averaged stress components in periodically arrayed Al lines with variations of passivation dielectrics for  $w/h$ : (a) 0.6 (b) 1.2, (c) 2.4, and (d) 23.5.

material properties, and correct boundary conditions is essential for calculating interconnect stress in passivated dense-metal line structure used in actual devices. Fig. 6 shows the variations of interconnect stress with four different passivation materials at each  $w/h$  value. For a very small line aspect ratio ( $w/h=23.5$ ), nearly biaxial stress state due to the small normal constraint by passivation and the dominated transverse constraint by the Si substrate was shown, which coincided with XRD-measured data for blanket Al stack film with passivations (cf. Fig. 4 or Table 2). For large line

Table 2

Summary of XRD-measured and FEM-calculated stresses of metal lines and films for various passivation dielectrics and line aspect ratios

Passivation dielectric	Analysis method	$\sigma_h$ (MPa)				$\sigma_x$ (MPa)	
		$w/h=0.6$	$w/h=1.2$	$w/h=2.4$	$w/h=23.5$	$w/h=23.5$	Blanket film
FOX	FEM	156	162	155	132	201	–
	XRD	115	121	127	119	175	200
FSG	FEM	512	462	341	148	216	–
	XRD	459	321	265	139	201	196
PETEOS	FEM	444	531	379	149	217	–
	XRD	327	441	353	134	195	208
PE-SiN	FEM	709	803	561	161	228	–
	XRD	611	728	512	145	204	207

aspect ratios ( $w/h < 2.4$ ), metal line stress was dominated by a normal constraint of passivation, which showed higher line stress for stiffer dielectrics. Therefore, the passivation stiffness dominantly affected the narrow line stress although four passivation dielectrics also differed in CTE and residual stress as shown in Fig. 3. But, it could again be seen that there was stress relaxation by a void or gap between metal lines for PE-SiN and PETEOS. That is, for  $w/h = 1.2, 2.4$ , there was a partial gap between the line (cf. Fig. 1) which led to a small decrease in stress for PETEOS and PE-SiN. For  $w/h = 0.6$ , there was total or partial gap between lines (cf. Fig. 1) which led to a large stress decrease for PETEOS and PE-SiN. Table 2 showed that there was reasonable correlation between the calculated and measured stress for passivated Al lines and films even though there were some different assumptions, limits, and errors included in each analysis methods. Hydrostatic stress is usually associated with stress-induced voiding because it requires a volume change in order to be reduced and drives the void formation and growth that can lead to interconnect failures [1,2,22]. The magnitude of tensile hydrostatic stress is therefore a good indication of the propensity of voiding damage [1,2] and even electromigration damage [22] in multilevel interconnect structure used in the actual device. Therefore, it is worth emphasizing that interconnect stress should be carefully measured or calculated by considering not only the passivation constraint effects but also its characteristic deposition shapes with the use of proper boundary conditions in numerical analysis.

#### 4. Conclusions

FEM-calculated volume-averaged stresses of Al–Cu interconnects were compared to XRD-measured values for various passivation dielectrics and metal line aspect ratios by considering not only the mechanical properties of passivation dielectrics but also their characteristic deposition shapes. Interconnect stress increased with increasing passivation stiffness and line aspect ratio due to the normal constraint by passivation dielectrics, while it was relaxed in narrow line passivated with voided or air-gapped dielectrics. A reasonable correlation between the measured and calculated stresses was found when a void or gap in dielectric between metal lines was taken into consideration in a numerical analysis. Therefore, using accurate material properties and correct boundary conditions by considering proper dielectric deposition characteristics is essential to obtain accurate interconnect stress in passivated metal line structures used in actual devices.

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